NL17SZYYXV5T2 Series

Product Preview

Pb Free Single Gate Device in SOT-553

The NL17SZYY is an ultra− high performance 2 Input NAND gate manufactured in 0.5 μm technology, fully functional to 1.65 V. Parts have the identical electrical specifications of the same device in the larger SC−88/SC−70 package. For full specification please see the ON Semiconductor web site: http://www.onsemi.com.

Devices to be available: NL17SZYYXV5T2 Series

00−2 Input NAND, Gate. 02 Input NOR Gate, 04 Single Inverter
U04 Unbuffered Single Inverter, 06 Single Inverter Open Drain (O.D.)
07− Single Buffer O.D., 08 2 Input AND Gate, 14− Single Schmitt INV
16− Single Input Buffer, 17 Single Schmitt Buffer,
32 2 Input OR Gate

Features

- Extremely High Speed: t_{PD} 2.2 ns (typ) @ V_{CC} = 3.0 V
- Designed for 1.65 V to 5.5 V Operation
- Over Voltage Tolerance (OVT) Input/Outputs
  Permits Logic Translation
- Balanced ±24 mA Output Drive @ V_{CC} = 3.3 V
- Near Zero Static Supply Current
- Ultra−Tiny SOT−553 5 Pin Package only 1.6 X 1.6 mm Footprint
  1/3 the Footprint Area of a SOT−23!
- Transistor count: 56
- Latchup Max Rating: > 200 mA
- Pin to Pin Replacement : TC7SZYYAFE

Typical Applications

- Cellular
- Digital Camera
- PDA
- Digital Video
- Bluetooth
- Micro−hard Drives

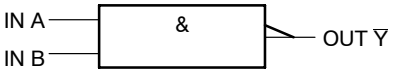

Figure 1. Logic Symbol

NOTE: The NL17SZ00XV5T2 is shown for illustration purposes.

ON Semiconductor®

http://onsemi.com

1.65 V to 5.5 V HIGH PERFORMANCE CMOS LOGIC

SOT−553
CASE 463B
PLASTIC

MARKING DIAGRAM

xx = Device Marking
D = One Digit Date Code

PIN ASSIGNMENT	
1	IN B
2	IN A
3	GND
4	OUT $\overline{Y}$
5	V_{CC}

FUNCTION TABLE

Inputs		Output
A	**B**	**$\overline{Y}$**
L	L	H
L	H	H
H	L	H
H	H	L

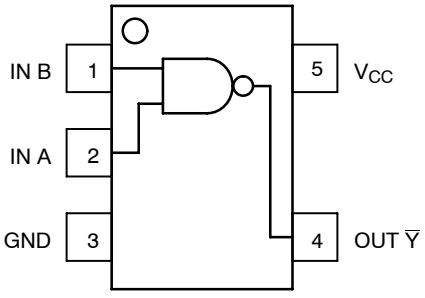

Figure 2. Pinout (Top View)

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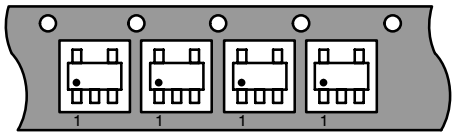
MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
V_{CC}	DC Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$		V
V_O	DC Output Voltage	$-0.5 \le V_O \le +7.0$	All Single Input Devices	V
		$-0.5 \le V_O \le V_{CC} + 0.5$	Outputs Active (Note 1)	V
I_{IK}	DC Input Diode Current	−50	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	−50	$V_O < GND$	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current Per Supply Pin	±100		mA
I_{GND}	DC Ground Current Per Ground Pin	±100		mA
T_{STG}	Storage Temperature Range	−65 to +150		°C

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum−rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

1. I_O absolute maximum rating must be observed.

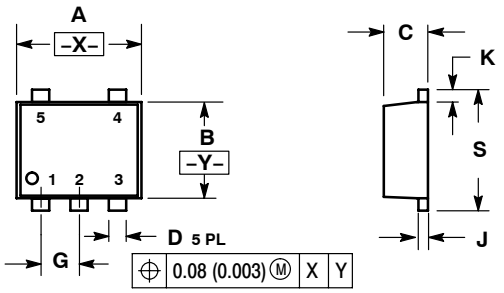


"T2" Pin One Away from Sprocket Hole (4k Reel)

Figure 3. SOT−553

PACKAGE DIMENSIONS

SOT−553, 5−LEAD
CASE 463B−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.50	1.70	0.059	0.067
B	1.10	1.30	0.043	0.051
C	0.50	0.60	0.020	0.024
D	0.17	0.27	0.007	0.011
G	0.50 BSC		0.020 BSC	
J	0.08	0.18	0.003	0.007
K	0.10	0.30	0.004	0.012
S	1.50	1.70	0.059	0.067

STYLE 1:
PIN 1. BASE 1
2. EMITTER 1/2
3. BASE 2
4. COLLECTOR 2
5. COLLECTOR 1

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE

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